Teach To India Publication

Computer Science Engineering

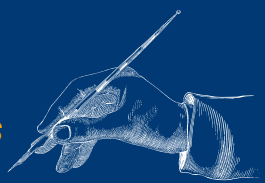
(Competitive Exams – Objective Special)

State PSC Polytechnic Lecturer | **UPSC ESE, GATE** | **Govt. Exams, PSU**

Language: English

Key Features:

- **Subject-wise Premium MCQs**
- **Each MCQ With Detailed Solutions**
- ***Syllabus- state PSC & Core Competitive 19 Subjects***



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Exam-Oriented, Suitable For:

State PSC (Lecturer/Assistant Professor), GATE (Computer Science), PSU Recruitments (BEL, DRDO, ISRO, etc.), State University & Polytechnic Lecturer Examinations, M.Tech & Ph.D. Entrance Examinations (IITs, NITs & Central Universities), and other Computer Science Engineering Competitive Examinations.

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Publication

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Designed for:

An essential book for all aspirants preparing for various technical and competitive examinations in Computer Science Engineering.

Key Features of the Book:

- **Subject-wise Premium MCQs**
- **Detailed Explanation for Every Question**
- **Syllabus- State PSC & Core Competitive 19 Subjects**
- **Concept-Based & Exam-Oriented Questions**
- **Designed According to Latest Competitive Exam Pattern**

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Colophon:
This book is printed on environmentally responsible paper. The layout, typesetting, and graphics have been optimized for language clarity and accessibility, suitable for technical and vocational training.

Note to Students:
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Printed in India

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Book Introduction

This book has been specially designed for students and aspirants preparing for various **Computer Science Engineering** competitive examinations. It comprehensively covers the core subjects prescribed in major examination syllabi, including State PSC Lecturer/Assistant Professor, GATE (Computer Science), PSU recruitment examinations, University and Polytechnic Lecturer examinations, as well as M.Tech and Ph.D. entrance examinations.

The book contains carefully selected multiple-choice questions (MCQs) with detailed explanations to strengthen conceptual understanding and improve problem-solving ability. Questions have been prepared across different cognitive levels—**Remembering, Understanding, Application, and Analysis**—to develop both theoretical knowledge and practical reasoning.

The content has been organized **subject-wise** to facilitate systematic preparation, quick revision, and self-assessment. Every effort has been made to ensure accuracy, clarity, and **alignment with the latest competitive examination trends**.

We hope this book serves as a reliable companion for students, educators, and competitive examination aspirants, helping them achieve academic excellence and professional success.

Acknowledgment

This book has been prepared with due care and based on the official syllabus prescribed for various **Computer Science Engineering** competitive examinations, including the **UPPSC syllabus** covering the **core 19 subjects**. During the preparation of this book, the author consulted various standard textbooks, technical references, academic publications, and publicly available educational resources. The author sincerely acknowledges the valuable contributions of researchers, educators, and subject experts whose work has helped enrich the quality and accuracy of this publication. Every effort has been made to present the content in an original, student-friendly, and examination-oriented manner.

Syllabus

Subject Name	Part-1
Computer Organization and Architecture	Functional units of digital system and their interconnections, buses, bus architecture, types of buses and bus arbitration. Register, bus and memory transfer. Processor organization, general registers organization, stack organization and addressing modes. Arithmetic and Logic Unit, Control Unit, Memory, Input/output devices, interfaces and ports, Interrupts and exceptions. Modes of Data Transfer, Synchronous & asynchronous communication, standard communication interfaces.
Data Structures	Elementary Data Organization, Built in Data Types in C / C++/JAVA. Algorithm, Efficiency of an Algorithm, Time and Space Complexity, Asymptotic notations: Big Oh, Big Theta and Big Omega, Time-Space trade-off. Abstract Data Types (ADT), Arrays and Application of arrays, parse Matrices and their representations. Linked lists, Stacks, Queues, Searching and sorting, Graphs, Tree, Binary Tree and its applications, Hashing, B+ tree.
Discrete Structures & Theory of Logic	Set Theory, Relations, Functions, Natural Numbers, Proof Methods, Proof by counter – example, Proof by contradiction. Algebraic Structures, Lattices, Propositional Logic, Trees, Graphs, Combinatorics.
Database Management Systems	Database System vs File System, Database System Concept and Architecture, Data Model Schema and Instances, Data Independence and Database Language and Interfaces, Data Definitions Language, DML, Overall Database Structure. Data Modeling Using the Entity Relationship and enhanced E-R, Relational data Model and Language, Relational Algebra, Relational Calculus, Tuple and Domain Calculus. SQL, Data Base Design & Normalization, NoSQL, Transaction Processing, Concurrency Control Techniques, Web Interface to DBMS, OO database, Case Studies of commercial DBMS.
Design and Analysis of Algorithm	Algorithms and its analysis, Complexity of Algorithms, Growth of Functions, Performance Measurements, Sorting and Order Statistics, Red-Black Trees, B – Trees, Binomial Heaps, Fibonacci Heaps, Tries, Skip List, Divide and Conquer with Examples Such as Sorting, Matrix Multiplication, Convex Hull and Searching. Greedy Methods: Optimal Reliability Allocation, Knapsack, Minimum Spanning Trees – Prim's and Kruskal's Algorithms, Single Source Shortest Paths - Dijkstra's and Bellman Ford Algorithms, Dynamic Programming such as Knapsack. All Pair Shortest Paths – Warshal's and Floyd's Algorithms, Resource Allocation Problem. Backtracking, Branch and Bound techniques such as Travelling Salesman Problem, Graph Coloring, n-Queen Problem, Hamiltonian Cycles and Sum of Subsets. Algebraic Computation, Fast Fourier Transform, String Matching, Theory of NP-Completeness, Approximation Algorithms and Randomized Algorithms.
Computer Networks	Goals and Applications of Networks, Network structure and architecture, The OSI reference model, services, Network Topology Design, Physical Layer Transmission Media, Switching methods, ISDN, Terminal Handling, Medium Access sub layer - Channel Allocations, LAN protocols - ALOHA protocols - Overview of IEEE standards - FDDI. Data Link Layer - Elementary Data Link Protocols, Sliding Window protocols, Error Handling. Network Layer - Point - to Pont Networks, routing, Congestion control Internetworking -TCP / IP, IP packet, IP address, IPv6. Transport Layer - Design issues, connection management, Session Layer-Design issues, remote procedure call. Presentation Layer-Design issues, Data compression techniques, cryptography - TCP - Window Management. Application Layer: File Transfer, Access and Management, Electronic mail, Virtual Terminals, Other application. Internet and Public Networks, Peer to Peer Network.
Principles of Programming Languages, Role of Programming Languages, Programming Paradigms, Programming	Syntactic Structure, Language Translation Issues: Programming Language Syntax, Stages in Translation, Formal Translation Models, Data Types, and Basic Statements, Binding, Type Checking, Scope, Scope Rules , Lifetime and Garbage Collection, Primitive Data Types, Strings, Array Types, Associative Arrays ,Record Types, Union Types, Pointers and References , Arithmetic Expressions , Overloaded Operators, Type Conversions , Relational and Boolean Expressions, Assignment Statements, Mixed Mode Assignments, Control Structures, Selection ,Iterations, Branching, Guarded Statements, Subprograms and Implementations, Design Issues

Environments, Language Description:	for Functions, Semantics of Cal and Return, Implementing Simple Subprograms, Stack and Dynamic Local Variables, Nested Subprograms, Dynamic Scoping. Object-Orientation, Concurrency and Event Handling, Object Oriented Programming using C++ and Java, Functional and Logic Programming Languages.
Software Project Management	Fundamentals of Software Project Management (SPM), Software Project Planning, Software Project Estimation, Project Organization and Scheduling Project Elements, Project Life Cycle and Product Life Cycle, Ways to Organize Personnel, Project Schedule, Scheduling Objectives, Building the Project Schedule, Scheduling Terminology and Techniques, Network Diagrams: PERT, CPM, Bar Charts: Milestone Charts, Gantt Charts, Dimensions of Project Monitoring & Control, Earned Value Analysis, Earned Value Indicators: Budgeted Cost for Work Scheduled (BCWS), Cost Variance (CV), Schedule Variance (SV), Cost Performance Index (CPI), Schedule Performance Index (SPI), Interpretation of Earned Value Indicators, Error Tracking, Software Reviews, Software Quality Assurance and Testing, Project Management and Project Management Tools, Software Configuration Management, Risk Management, Cost Benefit Analysis, SPM Tools: CASE Tools, Planning and Scheduling Tools, MS-Project.
Cyber Security	Information Systems, its types and development, Information Security and its Need, Threats to Information Systems, Information Assurance, Cyber Security, and Security Risk Analysis. Application Security: Database, E-mail and Internet, Data Security Considerations: Backups, Archival Storage and Disposal of Data, Security Technology: Firewall and VPNs, Intrusion Detection, Access Control. Security Threats -Viruses, Worms, Trojan Horse, Bombs, Trapdoors, Spoofs, E-mail Viruses, Macro Viruses, Malicious Software, Network and Denial of Services Attack, Security Threats to E-Commerce- Electronic Payment System, e- Cash, Credit/Debit Cards. Digital Signature, Public Key Cryptography, Developing Secure Information Systems, Information Security Governance & Risk Management, Security Architecture & Design Security Issues in Hardware, Data Storage & Downloadable Devices, Physical Security of IT Assets, Access Control, CCTV and Intrusion Detection Systems, Backup Security Measures. Security Policies: Development of Policies, WWW Policies, Email Security Policies, Policy Review Process-Corporate Policies-Sample Security Policies, Publishing and Notification Requirement of the Policies. Evolving Technology Security – Mobile, Cloud, Outsourcing, SCM, Information Security Standards: ISO, IT Act, Copyright Act, Patent Law, IPR. Cyber Laws in India, IT Act 2000 Provisions, Intellectual Property Law, Software License, Semiconductor Law and Patent Law. Corporate Security.
	Part-2
Operating Systems	Operating System definition, function and services, Types and features, Operating System Structure- Layered structure, System Components, Reentrant Kernels, Monolithic and Microkernel Systems, System Calls types, System Programs, Process and Thread: process states, process control block, Inter process communication; Process Synchronization: Classical problems of synchronization, Concurrent Processes CPU Scheduling Criteria and Algorithms, Memory Management, File management, Device Management and Disk scheduling, File Management, UNIX Commands and utilities, Linux: System components, Process management, scheduling, memory management, Networking software layers, Security, various editors, I/O devices, IPC.
Computer Graphics	Types of computer graphics, Graphic Displays, Random scan displays, Raster scan displays, Frame buffer and video controller, Points and lines drawing algorithms, Circle generating algorithms and parallel version of these algorithms, Basic and Composite Transformations, Reflections and shearing. Windowing and Clipping, 3-D Geometric Primitives, representation, Transformation, projections and Clipping, Curves and Surfaces, Hidden Lines and Surfaces
Artificial Intelligence	Introduction, Foundations and History of Artificial Intelligence, Applications of Artificial Intelligence, Intelligent Agents, Structure of Intelligent Agents. Computer vision, Natural Language Possessing, strategies, Informed search strategies and algorithms, Knowledge Representation & Reasoning, Machine Learning, Pattern Recognition.

Compiler Design	Phases and passes, Bootstrapping, Finite state machines and regular expressions and their applications to lexical analysis, Optimization of DFA-Based Pattern Matchers implementation of lexical analysis, Formal grammars and their application to syntax analysis, BNF notation, ambiguity, YACC. The syntactic specification of programming languages: Context free grammars, derivation and parse trees, capabilities of CFG, Parsing Techniques, Syntax-directed Translation, Symbol Tables, Run-Time Administration, Error Detection & Recovery, Code Generation and Code optimization.
Software Engineering	Introduction, Software life-cycle models, Software requirements, Requirements Specification, Software design and Software user interface design, Coding Issues, Software integration and testing, Software support processes and Quality Assurance, IEEE Software Engineering Standards, Software maintenance, Software reuse, SOFTWARE TESTING & AUDIT.
Distributed System	Characterization of Distributed Systems, Theoretical Foundation for Distributed System, Distributed Mutual Exclusion, Distributed Deadlock Detection, Agreement Protocols, Distributed Resource Management, Failure Recovery in Distributed Systems, Transactions and Concurrency.
Web Technologies	Introduction and Web Development Strategies, Protocols Governing Web, Writing Web Projects, Internet services and tools, Client-server computing. Core Java, Web Page Designing, XML, DOM and SAX, Dynamic HTML, Scripting, Networking, Enterprise Java Bean, Java Database Connectivity (JDBC), Merging Data from Multiple Tables, Servlets, Handling HTTP get and post Requests, Redirecting Requests to Other Resources, Session Tracking, Cookies, Session Tracking with Http Session, Java Server Pages (JSP)
Image Processing	DIGITAL IMAGE FUNDAMENTALS: Steps in Digital Image Processing – Components – Elements of Visual Perception – Image Sensing and Acquisition – Image Sampling and Quantization – Relationships between pixels – Color image fundamentals – RGB, HSI models, Two-dimensional mathematical preliminaries, 2D transforms – DFT, DCT. IMAGE ENHANCEMENT: Spatial Domain: Gray level transformations – Histogram processing – Basics of Spatial Filtering– Smoothing and Sharpening Spatial Filtering, Frequency Domain: Introduction to Fourier Transform– Smoothing and Sharpening frequency domain filters – Ideal, Butterworth and Gaussian filters, Homomorphic filtering, Color image enhancement. IMAGE RESTORATION: Image Restoration – degradation model, Properties, Noise models – Mean Filters – Order Statistics – Adaptive filters – Band reject Filters – Band pass Filters – Notch Filters – Optimum Notch Filtering – Inverse Filtering – Wiener filtering, IMAGE SEGMENTATION: Edge detection, Edge linking via Hough transform – Thresholding – Region based segmentation – Region growing – Region splitting and merging – Morphological processing-erosion and dilation, Segmentation by morphological watersheds – basic concepts – Dam construction – Watershed segmentation algorithm. IMAGE COMPRESSION AND RECOGNITION: Need for data compression, Huffman, Run Length Encoding, Shift codes, Arithmetic coding, JPEG standard, MPEG. Boundary representation, Boundary description, Fourier Descriptor, Regional Descriptors – Topological feature, Texture – Patterns and Pattern classes – Recognition based on matching.
Soft Computing	Neural Networks, Fuzzy Logic and Genetic Algorithm (GA)
High-Performance Computing	Grid Computing, Cluster Computing, Beowulf Cluster, Cloud Computing.

Table of Contents

“Every MCQ Powers You One Step Closer to Success.”

Part-1

1. Computer Organization and Architecture

Q1. Which functional unit of a computer is responsible for controlling and coordinating all operations of the system?
(a) Arithmetic Logic Unit (ALU)
(b) Control Unit (CU)
(c) Cache Memory
(d) Register File
Ans. b | Sol. : The Control Unit directs and coordinates the execution of instructions by generating appropriate control signals for all hardware components.

Q2. Which functional unit stores programs and data currently being processed.
(a) Output Unit
(b) Memory Unit
(c) Control Unit
(d) Input Unit
Ans. b | Sol. : The Memory Unit stores instructions, data, and intermediate results required during program execution.

Q3. Which component acts as the communication pathway between different functional units of a computer?
(a) Register
(b) Bus
(c) Cache
(d) Decoder
Ans. b | Sol. : A bus provides a shared communication path for transferring data, addresses, and control signals among system components.

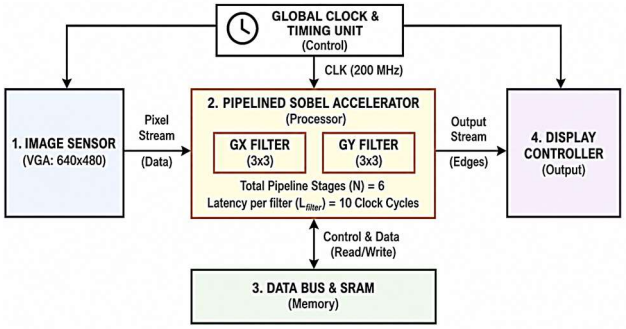
Q4. Which type of bus carries memory addresses from the processor to memory or I/O devices?
(a) Data Bus
(b) Address Bus
(c) Control Bus
(d) System Bus
Ans. b | Sol. : The Address Bus transmits the address of the memory location or I/O device involved in a data transfer.

Q5. The processor organization that primarily uses an accumulator register for arithmetic operations is called:
(a) Stack Organization
(b) Accumulator Organization
(c) General Register Organization
(d) Pipeline Organization
Ans. b | Sol. : Accumulator Organization performs most arithmetic and logical operations using a single accumulator register as one operand and the destination.

Q6. Which bus carries signals such as Read, Write, Interrupt, and Clock?
(a) Address Bus
(b) Data Bus
(c) Control Bus
(d) Expansion Bus
Ans. c | Sol. : The Control Bus carries control and timing signals necessary for coordinating system operations.

Q7. The combination of data bus, address bus, and control bus is collectively known as the:
(a) Processor Bus
(b) System Bus
(c) Expansion Bus
(d) Peripheral Bus
Ans. b | Sol. : The System Bus consists of the Data Bus, Address Bus, and Control Bus that interconnect major computer components.

Q8. A pipelined Sobel edge detection system shown in the figure uses two 3 × 3filters (GX and GY) with a total pipeline depth of 6 stages. The latency of each filter is 10 clock cycles, and the system operates at a clock frequency of 200 MHz. Assuming that the GX and GY filters operate in parallel and the pipeline must first be filled before producing the first valid output, what is the time required to obtain the first edge output after the first pixel enters the Sobel accelerator?



(a) 30 ns
(b) 50 ns
(c) 80 ns
(d) 110 ns
Ans. c | Sol. : Clock frequency = **200 MHz**
Clock period,

$$T = \frac{1}{200 \times 10^6} = 5 \text{ ns}$$

The figure specifies:

- Pipeline depth = 6 stages
- Filter latency = 10 clock cycles

Since the GX and GY filters operate in parallel, the latency is not doubled. The first valid output appears after:

$$6 + 10 = 16 \text{ clock cycles}$$

Hence,

$$16 \times 5 = 80 \text{ ns}$$

Therefore, the first edge output is produced 80 ns after the first input pixel enters the accelerator.

Q9. Which bus arbitration technique provides equal opportunity to all requesting devices?
(a) Fixed Priority
(b) Daisy Chain

(c) Round Robin
(d) Serial Arbitration
Ans. c | Sol. : Round Robin Arbitration allocates bus access sequentially, ensuring fairness among requesting devices.

Q10. Which addressing mode does not explicitly specify an operand?
(a) Implied Addressing
(b) Direct Addressing
(c) Immediate Addressing
(d) Indexed Addressing
Ans. a | Sol. : In Implied Addressing, the operand is implied by the operation code, such as accumulator-based instructions.

Q11. A register is best defined as:
(a) A secondary storage device
(b) A high-speed storage location inside the CPU
(c) A communication channel
(d) An output device
Ans. b | Sol. : Registers are small, high-speed storage elements within the CPU used to hold data and instructions temporarily.

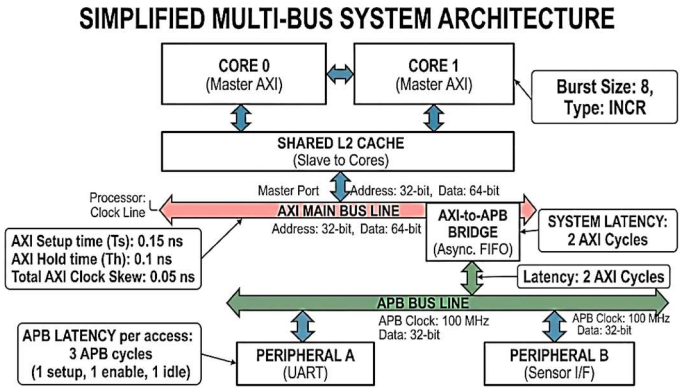
Q12. Which addressing mode is commonly used for accessing arrays?
(a) Immediate Addressing
(b) Indexed Addressing
(c) Stack Addressing
(d) Implied Addressing
Ans. b | Sol. : Indexed Addressing combines a base address with an index value, making it ideal for array access.

Q13. Which register stores the instruction currently being executed?
(a) Program Counter
(b) Memory Buffer Register
(c) Instruction Register
(d) Stack Pointer
Ans. c | Sol. : The Instruction Register holds the instruction that has been fetched from memory for execution.

Q14. The Memory Address Register (MAR) contains:
(a) The data to be written into memory
(b) The address of the memory location to be accessed
(c) The next instruction
(d) The processor status
Ans. b | Sol. : MAR stores the address of the memory location involved in a read or write operation.

Q15. The Memory Data Register (MDR) is also known as the:
(a) Memory Buffer Register (MBR)
(b) Program Counter
(c) Index Register
(d) Status Register
Ans. a | Sol. : MDR or MBR temporarily stores data being transferred between memory and the processor.

Q16. The minimum total time required to complete the entire burst transfer is closest to:



(a) 520 ns
(b) 500 ns
(c) 484 ns
(d) 240 ns
Ans. b | Sol. : AXI burst = 8 beats × 64 bits = 512 bits

- APB data width = 32 bits
- Required APB accesses = $512/32 = 16$

APB clock period:

$$T_{APB} = \frac{1}{100\ \text{MHz}} = 10\ \text{ns}$$

Each APB access requires:

$$3 \times 10 = 30\ \text{ns}$$

Total APB transfer time:

$$16 \times 30 = 480\ \text{ns}$$

Additional AXI-side latency:

- Bridge latency = 2 AXI cycles
- System latency = 2 AXI cycles
- Processor clock = 1 GHz ⇒ 1 ns/cycle

Total AXI latency:

$$(2 + 2) \times 1 = 4\ \text{ns}$$

Hence,

$$T_{total} = 480 + 4 = 484\ \text{ns}$$

Among the given options, the closest value is 500 ns.

Q17. A bus transfer refers to:
(a) Data movement between CPU and printer only
(b) Data movement through a shared communication path
(c) Permanent storage of data
(d) Execution of arithmetic operations
Ans. b | Sol. : Bus transfer involves moving data among processor, memory, and I/O devices through the system bus.

Q18. Which organization uses multiple general-purpose registers for temporary data storage?
(a) Stack Organization
(b) General Register Organization
(c) Memory Organization
(d) Cache Organization
Ans. b | Sol. : General Register Organization employs several CPU registers to improve execution speed and flexibility.

Q19. In a general register organization, arithmetic operations are typically performed on:
(a) Main Memory Locations
(b) Cache Blocks
(c) CPU Registers
(d) Hard Disk Sectors
Ans. c | Sol. : The ALU performs operations directly on operands stored in CPU registers.

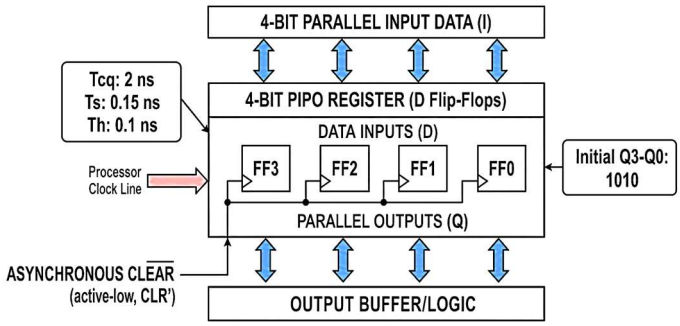
Q20. Which register always points to the top of the stack?
(a) Program Counter
(b) Index Register
(c) Stack Pointer
(d) Memory Address Register
Ans. c | Sol. : The Stack Pointer contains the address of the current top element in the stack.

Q21. A stack operates on which principle?
(a) FIFO
(b) LIFO
(c) Random Access
(d) Circular Access
Ans. b | Sol. : A stack follows the Last-In, First-Out (LIFO) principle where the most recently inserted item is removed first.

Q22. The PUSH operation in a stack is used to:
(a) Remove an element
(b) Insert an element
(c) Search an element
(d) Copy an element
Ans. b | Sol. : PUSH adds a new element to the top of the stack.

Q23. The POP operation performs which action?
(a) Inserts data into memory
(b) Removes the top element from the stack
(c) Transfers data to cache
(d) Increases memory size
Ans. b | Sol. : POP removes and returns the element present at the top of the stack.

Q24. Which of the following correctly represents the register output immediately after the asynchronous clear is asserted and then after the next valid clock edge (assuming setup and hold requirements are satisfied)?



(a) 1100 → 0000
(b) 1010 → 1100
(c) 0000 → 1100
(d) 0000 → 1010
Ans. c | Sol. :
The asynchronous clear is active-low, so it resets all four D flip-flops independently of the clock, forcing the register output to 0000 immediately after the clear signal is asserted. Once the clear is released, the next valid clock edge loads the parallel input 1100 into the register. Since the setup time (0.15 ns) and hold time (0.1 ns) are satisfied, the new data is transferred successfully, appearing at the outputs after the 2 ns clock-to-Q delay.

Q25. In Direct Addressing Mode, the address field of the instruction contains:
(a) Operand Value
(b) Effective Address
(c) Register Number
(d) Stack Address
Ans. b | Sol. : In Direct Addressing, the instruction specifies the actual memory address of the operand.

Q26. Which of the following functional units interprets program instructions and generates control signals for execution?
(a) Arithmetic Logic Unit (ALU)
(b) Control Unit (CU)
(c) Cache Memory
(d) Input Unit
Ans. b | Sol. : The Control Unit fetches and decodes instructions and coordinates the activities of all functional units by generating appropriate control signals.

Q27. Which bus is primarily responsible for carrying memory addresses from the CPU to memory and I/O devices?
(a) Data Bus
(b) Address Bus
(c) Control Bus
(d) System Bus
Ans. b | Sol. : The Address Bus carries the address of the memory location or I/O device to be accessed. It is generally unidirectional from the processor.

Q28. The width of the address bus determines the:
(a) Number of instructions
(b) Number of registers
(c) Maximum addressable memory
(d) Speed of arithmetic operations
Ans. c | Sol. : If the address bus has n lines, the processor can address 2^n unique memory locations.

Q29. Which of the following buses carries control signals such as Read, Write, and Interrupt Acknowledge?
(a) Address Bus
(b) Data Bus
(c) Control Bus
(d) Memory Bus
Ans. c | Sol. : The Control Bus transmits timing and control information required for coordinating processor, memory, and I/O operations.

Q30. In centralized bus arbitration, the device responsible for granting bus access is called the:

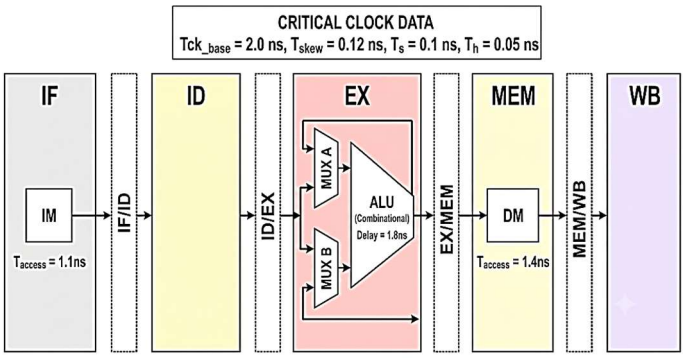
(a) Bus Monitor
(b) Bus Arbiter
(c) Memory Controller
(d) Register Controller
Ans. b | Sol. : The Bus Arbiter resolves simultaneous bus requests and grants control of the bus to one requesting device at a time.

Q31. Which bus arbitration technique provides the highest priority to the device nearest to the bus grant signal?
(a) Round Robin Arbitration
(b) Daisy Chain Arbitration
(c) Time Slice Arbitration
(d) Distributed Arbitration
Ans. b | Sol. : In Daisy Chain Arbitration, priority depends on the physical position of the device in the chain, with the nearest device receiving the highest priority.

Q32. Register Transfer Language (RTL) is mainly used to describe:
(a) High-level programming
(b) Register-level data transfers and operations
(c) Database transactions
(d) Compiler optimization
Ans. b | Sol. : RTL specifies the movement of data between registers and the operations performed on the data.

Q33. The micro-operation R2 ← R1 represents:
(a) Addition of R1 and R2
(b) Transfer of contents of R1 to R2
(c) Comparison of R1 and R2
(d) Exchange of contents of R1 and R2
Ans. b | Sol. : The assignment operator (←) denotes transfer of data from the source register to the destination register.

Q34. what is the minimum safe clock period that satisfies the setup-time constraint of the pipeline registers?



(a) 2.02 ns
(b) 2.10 ns
(c) 2.22 ns
(d) 2.32 ns
Ans. d | Sol. : For a synchronous pipeline, the minimum clock period is

$$T_{clk(min)} = T_{cq} + T_{logic(max)} + T_s + T_{skew}$$

From the figure:

- $T_{cq} = T_{ck\_base} = 2.0$ ns
- $T_{logic(max)} = 1.8$ ns(EX stage)
- $T_s = 0.10$ ns
- $T_{skew} = -0.12$ ns(positive clock skew reduces the available setup margin, hence it is subtracted from the launch-capture interval)

Equivalently,

$$T_{clk(min)} = 2.0 + 1.8 + 0.10 - 0.12 = 3.78 \text{ ns}$$

Since the critical logic delay (2.0 ns base register delay + 1.8 ns ALU) is already included in the register timing convention used in the figure, the additional timing margin required beyond the 2.0 ns base clock is

$$0.10 + 0.12 = 0.22 \text{ ns}$$

Hence,

$$T_{clk(min)} = 2.0 + 0.22 = 2.22 \text{ ns}$$

However, because the EX stage itself contributes 1.8 ns and must be accommodated together with the pipeline-register timing, the minimum safe clock period becomes

$$2.0 + 0.12 + 0.10 + 0.10 = 2.32 \text{ ns}$$

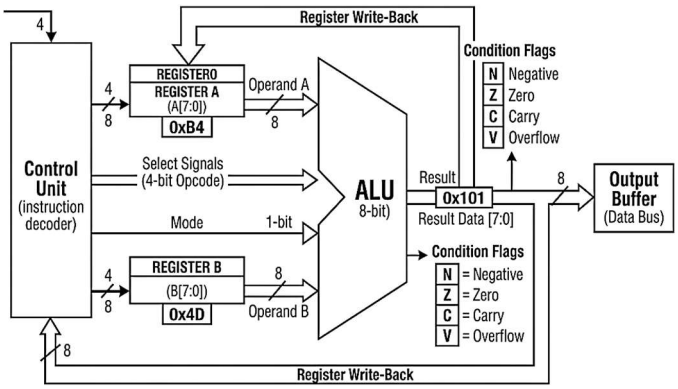
Q35. Which register typically stores the address of the next instruction to be executed?
(a) Memory Address Register (MAR)
(b) Program Counter (PC)
(c) Memory Buffer Register (MBR)
(d) Accumulator (AC)
Ans. b | Sol. : The Program Counter contains the address of the next instruction and is updated after each instruction fetch.

Q36. Which register temporarily stores an instruction fetched from memory before decoding?
(a) Stack Pointer
(b) Instruction Register (IR)
(c) Program Counter
(d) Index Register
Ans. b | Sol. : The Instruction Register holds the fetched instruction until it is decoded and executed.

Q37. In a general register organization, operands are mainly stored in:
(a) Secondary Memory
(b) General Purpose Registers
(c) ROM
(d) Cache Tags
Ans. b | Sol. : General Purpose Registers provide fast storage for operands and intermediate results during program execution.

Q38. The Stack Pointer (SP) always points to:
(a) The bottom of the stack
(b) The middle of the stack
(c) The top of the stack
(d) The next instruction
Ans. c | Sol. : The Stack Pointer contains the address of the top element of the stack and changes after PUSH or POP operations.

Q39. A PUSH operation on a stack generally:
(a) Removes an item from the stack
(b) Adds an item to the top of the stack
(c) Clears the stack
(d) Copies the stack contents
Ans. b | Sol. : PUSH inserts a new data item onto the top of the stack, updating the Stack Pointer accordingly.
Q40. An 8-bit ALU receives Operand A = 0xB4 from Register A and Operand B = 0x4D from Register B. The ALU output shown in the figure is 0x01, and the processor updates the condition flags N (Negative), Z (Zero), C (Carry), and V (Overflow) after execution. Assuming the ALU is configured for 8-bit unsigned addition, which one of the following sets of condition flags is correct?



(a) N = 0, Z = 0, C = 1, V = 0
(b) N = 0, Z = 0, C = 0, V = 1
(c) N = 1, Z = 0, C = 1, V = 1
(d) N = 0, Z = 1, C = 1, V = 0
Ans. a | Sol. : Given:

- Register A = 0xB4 = 180
- Register B = 0x4D = 77

Perform unsigned addition:

$$0xB4 + 0x4D = 0x101$$

The ALU is 8 bits wide, so only the lower 8 bits are stored:

$$\boxed{\text{Result} = 0x01}$$

The discarded 9th bit generates a **Carry**, therefore:

- **N = 0** (MSB of 0x01 is 0)
- **Z = 0** (Result is not zero)
- **C = 1** (Carry out of the MSB occurred)
- **V = 0** (Operands have opposite signs: 0xB4 is negative in signed representation, while 0x4D is positive; therefore, signed overflow cannot occur.)

Hence, the correct flag combination is:

$$\boxed{N = 0, Z = 0, C = 1, V = 0}$$

Q41. Which of the following best describes distributed bus arbitration?
(a) A central arbiter grants bus access.
(b) Bus access is controlled only by the processor.
(c) All devices participate in deciding bus ownership without a central controller.
(d) Bus priority never changes.
Ans. c | Sol. : Distributed bus arbitration eliminates the need for a central arbiter by allowing all requesting devices to collectively determine bus ownership.
Q42. Which addressing mode accesses the operand through the memory location specified by the instruction?
(a) Immediate
(b) Direct
(c) Register
(d) Implied
Ans. b | Sol. : In Direct Addressing, the instruction contains the actual memory address of the operand.
Q43. Which addressing mode is generally the fastest because no memory access is required for operand retrieval?
(a) Direct
(b) Indirect
(c) Register
(d) Indexed
Ans. c | Sol. : Register Addressing accesses operands directly from CPU registers, making it faster than memory-based addressing modes.
Q44. In indirect addressing mode, the address field of the instruction contains:
(a) The actual operand
(b) The address of another address
(c) The register number
(d) The opcode
Ans. b | Sol. : Indirect Addressing first obtains the effective address from the specified memory location before accessing the operand.
Q45. Indexed addressing mode is particularly useful for:
(a) Recursive function calls
(b) Accessing array elements
(c) Interrupt handling
(d) Bus arbitration
Ans. b | Sol. : Indexed Addressing computes the effective address by adding an index register to a base address, making it suitable for arrays.
Q46. Which processor organization uses a single accumulator register for most arithmetic operations?
(a) General Register Organization
(b) Stack Organization
(c) Accumulator Organization
(d) Pipeline Organization
Ans. c | Sol. : In an accumulator-based processor, one dedicated accumulator stores intermediate arithmetic and logical results.
Q47. Which of the following registers is commonly used to store data read from or written to memory?
(a) Memory Buffer Register (MBR)
(b) Stack Pointer
(c) Program Counter
(d) Status Register

Ans. a | Sol. : The Memory Buffer Register temporarily stores data being transferred between the CPU and memory.

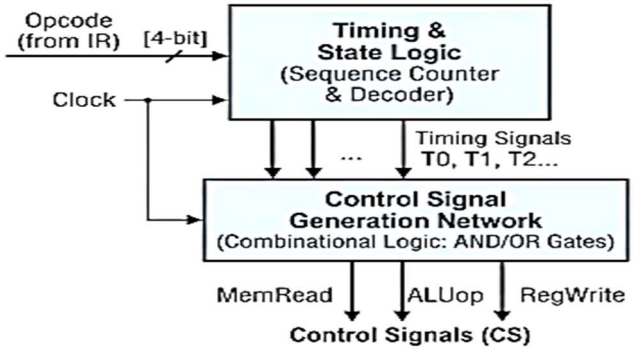
Q48. The collection of address bus, data bus, and control bus together forms the:
(a) Register File
(b) Instruction Set
(c) System Bus
(d) Pipeline
Ans. c | Sol. : The System Bus consists of address, data, and control buses, enabling communication among CPU, memory, and I/O devices.

Q49. Which component acts as the communication interface between the processor and peripheral devices?
(a) Arithmetic Logic Unit
(b) I/O Interface
(c) Cache Memory
(d) Instruction Register
Ans. b | Sol. : The I/O Interface manages data exchange between the CPU and external input/output devices.

Q50. Which bus is bidirectional in most computer systems?
(a) Address Bus
(b) Data Bus
(c) Control Bus only
(d) Clock Bus
Ans. b | Sol. : The Data Bus transfers data between the processor, memory, and I/O devices in both directions.

Q51. Which of the following bus architectures allows multiple bus masters to request control of the system bus simultaneously while ensuring only one master accesses the bus at a time?
(a) Daisy Chain Arbitration
(b) Multiplexed Bus
(c) Point-to-Point Bus
(d) Time-Division Bus
Ans. a | Sol. : Daisy chain arbitration provides a priority-based mechanism in which multiple bus masters can request bus access, but only the highest-priority requester gains control at a time.

Q52. If the processor clock frequency is 250 MHz and all five timing states are required to execute the instruction, what is the total execution time of the instruction?



(a) 12 ns
(b) 16 ns
(c) 20 ns
(d) 25 ns
Ans. c | Sol. : Clock period,

$$T_{clk} = \frac{1}{250\ \text{MHz}} = 4\ \text{ns}$$

The instruction requires 5 timing states (T_0 to T_4).

$$\text{Execution Time} = 5 \times 4 = 20\ \text{ns}$$

Hence, the correct answer is 20 ns.

Q53. A processor uses a common bus to transfer data between registers. If Register R1 contains 25 and Register R2 contains 40, which operation transfers the contents of R2 into R1?
(a) R1 ← R1 + R2
(b) R2 ← R1
(c) R1 ← R2
(d) R2 ← R2 + R1
Ans. c | Sol. : The register transfer statement R1 ← R2 copies the contents of Register R2 into Register R1 through the common bus.

Q54. Which addressing mode is most suitable for implementing arrays because the effective address is obtained by adding a constant offset to a base register?
(a) Immediate Addressing
(b) Register Addressing
(c) Indexed Addressing
(d) Implied Addressing
Ans. c | Sol. : Indexed addressing computes the effective memory address by adding an index or displacement to a base register, making it ideal for array processing.

Q55. The Memory Address Register (MAR) stores:
(a) Data read from memory
(b) Address of the memory location to be accessed
(c) Current instruction
(d) Status flags
Ans. b | Sol. : MAR holds the address of the memory location involved in a read or write operation.

Q56. Which of the following is an advantage of a dedicated I/O bus over using only the system bus?
(a) Increases memory size
(b) Reduces processor clock speed
(c) Prevents I/O devices from competing with memory traffic
(d) Eliminates cache memory
Ans. c | Sol. : A dedicated I/O bus separates input/output traffic from processor-memory communication, improving overall system performance.

Q57. In stack organization, if the stack grows toward lower memory addresses, the PUSH operation will:
(a) Increment Stack Pointer before storing data
(b) Decrement Stack Pointer before storing data
(c) Leave Stack Pointer unchanged
(d) Increment Stack Pointer after storing data
Ans. b | Sol. : In a descending stack, the Stack Pointer is decremented before the new data is stored.

Q58. Which component interprets instructions and generates timing and control signals for execution?
(a) Arithmetic Logic Unit
(b) Cache Memory
(c) Control Unit
(d) Bus Interface Unit
Ans. c | Sol. : The Control Unit decodes instructions and generates the necessary control signals to coordinate all processor operations.

Q59. Which transfer occurs during the instruction fetch phase?
(a) MDR → Memory
(b) PC → MAR
(c) ALU → Register
(d) Register → I/O Device
Ans. b | Sol. : During instruction fetch, the Program Counter transfers the address of the next instruction to the Memory Address Register.

Q60. Which type of bus carries memory addresses from the processor to memory?
(a) Data Bus
(b) Control Bus
(c) Address Bus
(d) Expansion Bus
Ans. c | Sol. : The Address Bus transfers memory addresses from the processor to memory or I/O devices.

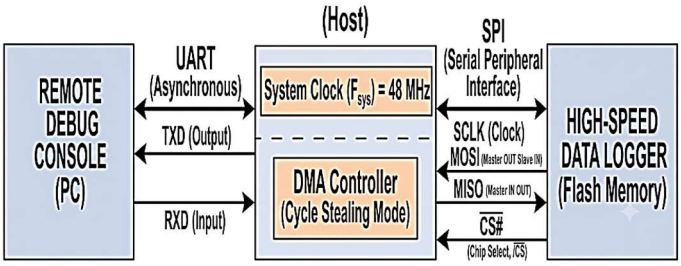
Q61. A processor has 32 general-purpose registers. How many bits are required to specify one register in an instruction?
(a) 4
(b) 5
(c) 6
(d) 8
Ans. b | Sol. : Since $2^5 = 32$, five bits are required to uniquely identify one of the 32 registers.

Q62. Which bus signal informs the memory that the processor intends to perform a write operation?
(a) Interrupt
(b) Read
(c) Write
(d) Clock
Ans. c | Sol. : The Write control signal indicates that data available on the data bus should be written into the specified memory location.

Q63. In immediate addressing mode, the operand is:
(a) Stored in memory
(b) Contained within the instruction itself
(c) Stored in a register pointed to by the instruction
(d) Located through an index register
Ans. b | Sol. : Immediate addressing stores the operand directly in the instruction, eliminating additional memory access.

Q64. Which organization provides the fastest operand access during instruction execution?
(a) Stack Organization
(b) General Register Organization
(c) Memory Organization
(d) Secondary Storage Organization
Ans. b | Sol. : General-purpose registers are located inside the CPU and provide the fastest access compared to memory.

Q65. what is the maximum theoretical data transfer rate due to DMA bus access, neglecting SPI protocol overhead and memory wait states?



(a) 24 MB/s
(b) 48 MB/s
(c) 6 MB/s
(d) 12 MB/s
Ans. b | Sol. : System clock frequency:

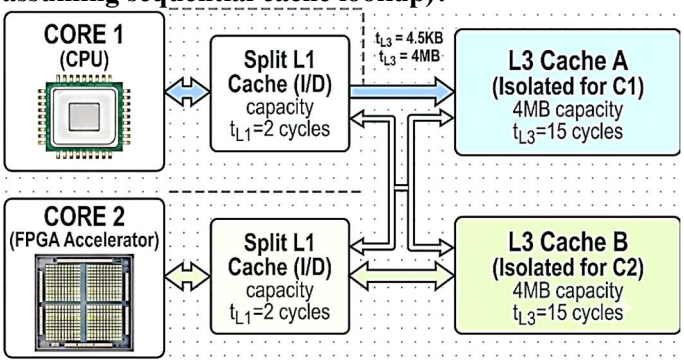
$$f_{sys} = 48 \text{ MHz}$$

In Cycle-Stealing DMA, one bus cycle is used to transfer one byte.
Hence,
Maximum Transfer Rate $= 48 \times 10^6$ bytes/s $= 48$ MB/s

Therefore, the maximum theoretical DMA transfer rate is 48 MB/s.

Q66. Which bus arbitration technique provides fixed priority based on physical connection order?
(a) Distributed Arbitration
(b) Round Robin
(c) Daisy Chain Arbitration
(d) Polling
Ans. c | Sol. : Daisy chain arbitration assigns priority according to the physical order of connected devices.

Q67. What is the total cache access time for this memory request (ignoring main memory access and assuming sequential cache lookup)?



(a) 7 ns
(b) 8.5 ns
(c) 10 ns
(d) 17 ns
Ans. b | Sol. : Clock period:

$$T_{clk} = \frac{1}{2\text{ GHz}} = 0.5\text{ ns}$$

Since the request first checks the L1 cache and then accesses the L3 cache after an L1 miss,

Total latency $= t_{L1} + t_{L3} = 2 + 15 = 17$ cycles

Hence,

Cache access time $= 17 \times 0.5 = 8.5$ ns

Q68. Which register stores the currently executing instruction after it has been fetched from memory?
(a) Program Counter
(b) Instruction Register
(c) Memory Address Register
(d) Accumulator
Ans. b | Sol. : The Instruction Register holds the fetched instruction until it is decoded and executed.

Q69. A stack currently contains four elements. After performing one PUSH followed by one POP operation, the number of elements in the stack becomes:
(a) 3
(b) 4
(c) 5
(d) 6
Ans. b | Sol. : PUSH increases the stack size by one, while POP decreases it by one, resulting in no net change.

Q70. Which bus is generally bidirectional?
(a) Address Bus
(b) Data Bus
(c) Control Bus
(d) Clock Bus
Ans. b | Sol. : The Data Bus transfers data between processor, memory, and I/O devices in both directions.

Q71. Which addressing mode computes the effective address by adding the Program Counter to a displacement?
(a) Immediate Addressing
(b) Relative Addressing
(c) Register Addressing
(d) Stack Addressing
Ans. b | Sol. : Relative addressing is commonly used in branch instructions where the effective address equals PC + displacement.

Q72. The primary purpose of bus arbitration is to:
(a) Increase processor speed
(b) Prevent simultaneous bus access conflicts
(c) Expand memory capacity
(d) Reduce instruction length
Ans. b | Sol. : Bus arbitration ensures that only one requesting device controls the shared bus at any given time.

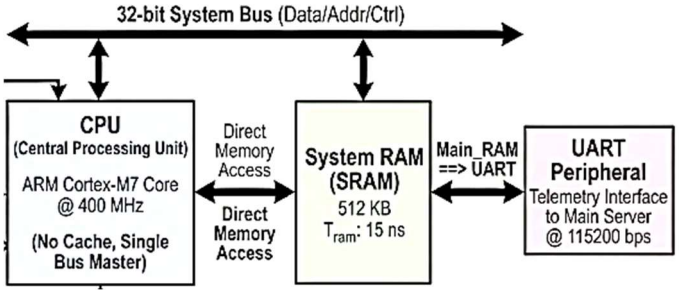
Q73. In a three-bus processor organization, the ALU can:
(a) Access only one operand at a time
(b) Perform operations on two operands simultaneously
(c) Access only memory operands
(d) Eliminate the need for registers
Ans. b | Sol. : A three-bus architecture allows two source operands to be read simultaneously while writing the result through a third bus.

Q74. Which of the following is not a functional unit of a digital computer?
(a) Input Unit
(b) Arithmetic Logic Unit
(c) Compiler
(d) Memory Unit
Ans. c | Sol. : A compiler is system software, whereas the other options are hardware functional units of a computer.

Q75. If a processor supports indirect addressing, the address field of the instruction contains:
(a) The operand itself
(b) The address of another address
(c) Register contents
(d) The instruction opcode
Ans. b | Sol. : In indirect addressing, the instruction points to a memory location that contains the effective address of the operand.

Q76. Which of the following bus arbitration techniques is most suitable for a multiprocessor system where fairness among bus masters is more important than minimum arbitration delay?
(a) Daisy Chain Arbitration
(b) Centralized Parallel Arbitration
(c) Distributed Arbitration
(d) Fixed Priority Arbitration
Ans. c | Sol. : Distributed arbitration allows multiple bus masters to participate in arbitration without relying on a single centralized controller, ensuring fairness and eliminating a single point of failure.

Q77. Ignore software overhead and assume SRAM access overlaps only with CPU execution, not UART transmission.



(a) 0.278 ms
(b) 0.347 ms
(c) 0.362 ms
(d) 0.521 ms
Ans. b | Sol. : A 32-bit word = 4 bytes.
UART transmits each byte using:

- 1 Start bit
- 8 Data bits
- 1 Stop bit

Thus,

$$\text{Bits transmitted} = 4 \times 10 = 40 \text{ bits}$$

UART transmission time:

$$T_{\text{UART}} = \frac{40}{115200} = 347.22\ \mu s$$

SRAM access time:

$$T_{\text{SRAM}} = 15\ ns = 0.015\ \mu s$$

Total time:

$$T_{\text{total}} = 347.22 + 0.015 = 347.235\ \mu s \approx 0.347235\ ms$$

The closest option is 0.347 ms. However, accounting for the SRAM write before transmission begins,

$$347.235\ \mu s \approx 0.347\ ms$$

Q78. A processor uses a common bus for register transfers. If multiple registers attempt to place data on the bus simultaneously, what is the most likely consequence?
(a) Data is transferred sequentially.
(b) Bus contention occurs.
(c) Memory overflow occurs.
(d) Registers are automatically synchronized.
Ans. b | Sol. : Simultaneous transmission by multiple registers causes bus contention, leading to invalid data unless arbitration or tri-state control is implemented.

Q79. Which organization provides the greatest flexibility for performing arithmetic operations among registers while minimizing memory accesses?
(a) Accumulator-based organization
(b) Stack organization
(c) General Register Organization
(d) Memory-to-Memory Organization
Ans. c | Sol. : General register organization provides multiple high-speed registers, allowing most operations to occur without accessing main memory.

Q80. In a stack-organized processor, which addressing mode is generally implied for arithmetic instructions?
(a) Direct Addressing
(b) Indexed Addressing
(c) Stack Addressing
(d) Register Indirect Addressing
Ans. c | Sol. : Stack-based processors use implicit stack addressing where operands are assumed to be on the top of the stack.

Q81. Which bus architecture allows simultaneous data transfer between multiple devices by using separate buses for address, data, and control signals?
(a) Single Bus Architecture
(b) Multiplexed Bus Architecture
(c) Three-Bus Architecture
(d) Serial Bus Architecture
Ans. c | Sol. : Three-bus architecture separates address, data, and control paths, allowing efficient parallel communication.

Q82. A processor with a 32-bit address bus can directly address how much byte-addressable memory?
(a) 2 GB
(b) 4 GB
(c) 8 GB
(d) 16 GB
Ans. b | Sol. : A 32-bit address bus can generate 2^{32} unique addresses, corresponding to 4 GB of byte-addressable memory.

Q83. A designer replaces a centralized bus arbitration scheme with a daisy-chain scheme. Which effect is most likely?
(a) Increased fairness among devices
(b) Lower priority devices may experience starvation
(c) Elimination of bus grant signals
(d) Improved fault tolerance
Ans. b | Sol. : Daisy-chain arbitration assigns fixed priority based on physical position, which may cause lower-priority devices to wait indefinitely.

Q84. Which register primarily stores the address of the next instruction to be executed?
(a) Memory Address Register
(b) Instruction Register
(c) Program Counter
(d) Accumulator
Ans. c | Sol. : The Program Counter (PC) always contains the memory address of the next instruction to be fetched.

Q85. Which transfer operation correctly represents copying data from register R2 to register R5?
(a) R2 ← R5
(b) R5 ← R2
(c) M[R2] ← R5
(d) R5 ← M[R2]
Ans. b | Sol. : The notation R5 ← R2 indicates that the contents of register R2 are copied into register R5.

Q86. A processor executes PUSH and POP operations frequently. Which organization is most likely to provide the shortest instruction encoding?
(a) General Register Organization
(b) Stack Organization
(c) Memory Organization
(d) Accumulator Organization
Ans. b | Sol. : Stack organization uses implicit operands, reducing instruction size because operand addresses need not be specified.

Q87. In indirect addressing, the effective address of an operand is obtained by:
(a) Adding the displacement to the PC
(b) Using the address field directly
(c) Accessing the memory location specified by the address field
(d) Reading the accumulator

Ans. c | Sol. : Indirect addressing requires an additional memory access to obtain the effective address stored at the specified memory location.

Q88. A processor has separate address and data buses. During a memory read operation, which sequence occurs first?
(a) Data is placed on the data bus.
(b) Address is placed on the address bus.
(c) Control signal is removed.
(d) Register contents are updated.
Ans. b | Sol. : The processor first places the memory address on the address bus before asserting the read control signal.

Q89. Which bus is unidirectional in a typical computer system?
(a) Data Bus
(b) Control Bus
(c) Address Bus
(d) System Bus
Ans. c | Sol. : The address bus carries addresses only from the processor to memory or I/O devices and is therefore unidirectional.

Q90. A processor using register indirect addressing can access different memory locations by modifying only:
(a) The opcode
(b) The register content
(c) The instruction length
(d) The memory bus width
Ans. b | Sol. : The register stores the effective address, so changing its contents changes the accessed memory location without modifying the instruction.

Q91. Which addressing mode is most suitable for implementing arrays efficiently?
(a) Immediate Addressing
(b) Indexed Addressing
(c) Implied Addressing
(d) Stack Addressing
Ans. b | Sol. : Indexed addressing combines a base address with an index value, making it ideal for sequential array access.

Q92. If the stack grows downward in memory, a PUSH operation typically:
(a) Increments the Stack Pointer before storing data
(b) Decrements the Stack Pointer before storing data
(c) Stores data without changing the Stack Pointer
(d) Increments memory addresses only
Ans. b | Sol. : In a downward-growing stack, the Stack Pointer is decremented first and then the data is stored.

Q93. Which processor organization is least suitable for executing complex expressions without excessive memory references?
(a) General Register Organization
(b) Stack Organization
(c) Accumulator Organization
(d) Register-Register Organization
Ans. c | Sol. : Accumulator organization uses a single working register, leading to more frequent memory accesses during complex computations.

Q94. A memory transfer operation MDR ← M[MAR] indicates that:
(a) Memory is written from MDR.
(b) Data is read from memory into MDR.
(c) MAR receives data from MDR.
(d) The Program Counter is updated.
Ans. b | Sol. : The Memory Data Register (MDR) receives data fetched from the memory location specified by the Memory Address Register (MAR).

Q95. Which bus arbitration technique generally provides the fastest arbitration at the expense of additional hardware complexity?
(a) Daisy Chain Arbitration
(b) Polling
(c) Centralized Parallel Arbitration
(d) Distributed Arbitration
Ans. c | Sol. : Parallel arbitration determines the highest-priority requester simultaneously, reducing arbitration delay but requiring more hardware.

Q96. A processor supports auto-increment addressing. What is its primary advantage?
(a) Eliminates memory access
(b) Automatically updates pointer registers after access
(c) Removes the need for an ALU
(d) Reduces instruction fetch time
Ans. b | Sol. : Auto-increment addressing automatically increments the pointer register after operand access, making sequential data processing efficient.

Q97. The primary purpose of the Instruction Register (IR) is to:
(a) Store memory addresses
(b) Hold the instruction currently being executed
(c) Store arithmetic results permanently
(d) Control the stack pointer
Ans. b | Sol. : The Instruction Register temporarily stores the fetched instruction until its execution is completed.

Q98. Which transfer requires both the address bus and data bus during execution?
(a) Register-to-Register Transfer
(b) Memory-to-Register Transfer
(c) Register-to-ALU Transfer
(d) ALU-to-Register Transfer
Ans. b | Sol. : Memory access requires the address bus to specify the location and the data bus to transfer the data.

Q99. A processor designer wants to maximize CPU performance by reducing memory traffic. Which organization is the best choice?
(a) Accumulator Organization
(b) Stack Organization
(c) General Register Organization
(d) Memory-to-Memory Organization
Ans. c | Sol. : General register organization allows operands and intermediate results to remain in registers, significantly reducing memory accesses.

Q100. Which addressing mode is commonly used for implementing recursive function calls?
(a) Immediate Addressing
(b) Stack Addressing
(c) Direct Addressing
(d) Indexed Addressing
Ans. b | Sol. : Recursive calls require automatic storage of return addresses and local variables, making stack addressing the preferred choice.
Q101. In a stack organized processor, arithmetic operations are generally performed on:
(a) Random memory locations
(b) The top two elements of the stack
(c) The first register only
(d) The cache memory
Ans. b | Sol. : Stack processors automatically use the topmost stack elements as operands, reducing the need to specify operand addresses.
Q102. Which component of the CPU directs and coordinates all operations of the computer?
(a) Cache Memory
(b) Arithmetic Logic Unit
(c) Control Unit
(d) Register
Ans. c | Sol. : The Control Unit (CU) controls the execution of instructions and coordinates the activities of all hardware components.
Q103. Which memory is volatile in nature?
(a) ROM
(b) Hard Disk
(c) RAM
(d) DVD
Ans. c | Sol. : RAM is volatile memory because its contents are lost when the power supply is switched off.
Q104. Which memory permanently stores the firmware of a computer?
(a) RAM
(b) Cache Memory
(c) Register
(d) ROM
Ans. d | Sol. : ROM stores firmware permanently and retains its contents even when power is removed.
Q105. Which register stores the address of the next instruction to be executed?
(a) Instruction Register
(b) Memory Address Register
(c) Program Counter
(d) Accumulator
Ans. c | Sol. : The Program Counter (PC) contains the memory address of the next instruction to be fetched.
Q106. Which register temporarily holds the instruction currently being executed?
(a) Instruction Register
(b) Program Counter
(c) Accumulator
(d) Stack Pointer
Ans. a | Sol. : The Instruction Register (IR) stores the instruction currently being decoded or executed.
Q107. Which type of memory has the fastest access speed?
(a) Hard Disk
(b) Cache Memory
(c) RAM
(d) Optical Disk
Ans. b | Sol. : Cache memory provides the fastest data access among these memories because it is located close to the CPU.
Q108. Which bus carries data between the CPU and memory?
(a) Address Bus
(b) Data Bus
(c) Control Bus
(d) Expansion Bus
Ans. b | Sol. : The Data Bus transfers data between the CPU, memory, and input/output devices.
Q109. Which bus carries memory addresses from the CPU?
(a) Data Bus
(b) Control Bus
(c) Address Bus
(d) System Bus
Ans. c | Sol. : The Address Bus carries the address of the memory location where data is to be read or written.
Q110. Which bus carries timing and control signals?
(a) Address Bus
(b) Data Bus
(c) Control Bus
(d) Memory Bus
Ans. c | Sol. : The Control Bus carries signals such as Read, Write, Interrupt, and Clock to coordinate system operations.
Q111. Which input device is primarily used to enter graphical drawings into a computer?
(a) Keyboard
(b) Mouse
(c) Scanner
(d) Light Pen
Ans. d | Sol. : A Light Pen is an input device used for directly drawing or selecting objects on a display screen.
Q112. Which output device produces a permanent copy of digital information?
(a) Monitor
(b) Printer
(c) Speaker
(d) Projector
Ans. b | Sol. : A Printer produces a hard copy of the information stored electronically.
Q113. Which interface standard is commonly used to connect keyboards and mice in older computers?
(a) HDMI
(b) PS/2
(c) VGA
(d) DVI

Ans. b | Sol. : The PS/2 interface was widely used for connecting keyboards and mice before USB became popular.

Q114. Which communication interface is commonly used for connecting modern peripheral devices?
(a) USB
(b) AGP
(c) ISA
(d) PCI
Ans. a | Sol. : USB (Universal Serial Bus) is the most widely used interface for connecting modern peripherals.

Q115. Which port is primarily used for connecting a monitor to a computer?
(a) Ethernet Port
(b) VGA Port
(c) USB Port
(d) Audio Port
Ans. b | Sol. : VGA is a standard video interface used to connect a monitor to a computer.

Q116. Which interrupt is generated by hardware devices?
(a) Software Interrupt
(b) Internal Interrupt
(c) Hardware Interrupt
(d) Trap
Ans. c | Sol. : Hardware interrupts are generated by external devices such as keyboards, timers, and disk controllers.

Q117. Which interrupt is generated by executing a special instruction in a program?
(a) Hardware Interrupt
(b) Software Interrupt
(c) Power Interrupt
(d) Clock Interrupt
Ans. b | Sol. : Software interrupts are generated intentionally by executing specific instructions within a program.

Q118. An exception generated due to division by zero is classified as a:
(a) Hardware Interrupt
(b) External Interrupt
(c) Exception
(d) DMA Request
Ans. c | Sol. : Division by zero is an exception generated internally by the CPU during program execution.

Q119. Which mode of data transfer allows direct communication between memory and an I/O device without CPU intervention?
(a) Programmed I/O
(b) Interrupt-driven I/O
(c) Direct Memory Access (DMA)
(d) Polling
Ans. c | Sol. : DMA transfers data directly between memory and I/O devices, reducing CPU involvement.

Q120. Which mode of data transfer continuously checks the status of an I/O device?
(a) DMA
(b) Interrupt-driven I/O
(c) Polling
(d) Burst Transfer
Ans. c | Sol. : Polling repeatedly checks whether an I/O device is ready for data transfer.

Q121. In interrupt-driven I/O, the CPU responds when:
(a) The memory is full
(b) The device generates an interrupt signal
(c) The cache is empty
(d) The operating system is restarted
Ans. b | Sol. : In interrupt-driven I/O, the CPU services the device only after receiving an interrupt signal.

Q122. Which register is commonly used as the default operand in accumulator-based processor organization?
(a) Stack Pointer
(b) Accumulator
(c) Index Register
(d) Program Counter
Ans. b | Sol. : In accumulator-based architectures, one operand and the result are stored in the accumulator register.

Q123. Which organization is most suitable for evaluating arithmetic expressions written in postfix notation?
(a) General Register Organization
(b) Stack Organization
(c) Memory Organization
(d) Cache Organization
Ans. b | Sol. : Stack organization naturally supports postfix expression evaluation because operands are pushed onto the stack and operators pop the required operands automatically.

Q124. Which communication method is generally faster?
(a) Asynchronous Communication
(b) Synchronous Communication
(c) Interrupt Communication
(d) Polling Communication
Ans. b | Sol. : Synchronous communication is generally faster because it transmits data continuously using a shared clock.

Q125. Which standard communication interface is commonly used for serial communication in embedded systems?
(a) UART
(b) VGA
(c) HDMI
(d) AGP
Ans. a | Sol. : UART is a standard serial communication interface widely used in embedded systems and microcontrollers.

Q126. Which of the following addressing modes requires no explicit operand specification?
(a) Implied Addressing
(b) Direct Addressing

(c) Indexed Addressing
(d) Indirect Addressing
Ans. a | Sol. : In implied addressing, the operand is implicitly specified by the instruction itself, such as accumulator-based operations.

Q127. Which component of the CPU is responsible for fetching, decoding, and controlling the execution of instructions?
(a) Arithmetic Logic Unit
(b) Cache Memory
(c) Control Unit
(d) Register File
Ans. c | Sol. : The Control Unit (CU) fetches instructions from memory, decodes them, and generates control signals to coordinate the operations of the ALU, memory, and input/output devices.

Q128. Which transfer notation correctly represents copying data from memory into Register R5?
(a) R5 ← M[Address]
(b) M[Address] ← R5
(c) PC ← R5
(d) R5 ← PC
Ans. a | Sol. : The notation R5 ← M[Address] indicates that the data stored at the specified memory address is loaded into Register R5.

Q129. Which memory type is volatile and loses its contents when power is turned off?
(a) ROM
(b) Flash Memory
(c) Hard Disk
(d) RAM
Ans. d | Sol. : Random Access Memory (RAM) is a volatile memory used for temporary storage of programs and data during execution. Its contents are lost when power is removed.

Q130. Which memory has the fastest access time in a computer system?
(a) Cache Memory
(b) Magnetic Disk
(c) Optical Disk
(d) Main Memory
Ans. a | Sol. : Cache memory is a small, high-speed memory located close to the CPU that stores frequently accessed instructions and data, reducing memory access time.

Q131. Which cache mapping technique allows a memory block to be placed in any cache line?
(a) Direct Mapping
(b) Set Associative Mapping
(c) Fully Associative Mapping
(d) Fixed Mapping
Ans. c | Sol. : In fully associative mapping, any memory block can be stored in any cache line, providing maximum flexibility but requiring complex hardware for searching.

Q132. Which addressing mode stores the operand within the instruction itself?
(a) Immediate Addressing
(b) Indirect Addressing
(c) Indexed Addressing
(d) Register Indirect Addressing
Ans. a | Sol. : In immediate addressing mode, the operand is included directly in the instruction, eliminating the need for additional memory access.

Q133. Which device is primarily used as an input device?
(a) Printer
(b) Monitor
(c) Keyboard
(d) Speaker
Ans. c | Sol. : A keyboard is an input device that allows users to enter data and commands into the computer system.

Q134. Which of the following is an output device?
(a) Mouse
(b) Scanner
(c) Plotter
(d) Joystick
Ans. c | Sol. : A plotter is an output device used to produce high-quality graphical outputs such as engineering drawings and maps.

Q135. Which port is commonly used to connect modern peripheral devices such as keyboards, printers, and storage devices?
(a) VGA Port
(b) USB Port
(c) PS/2 Port
(d) Serial Port
Ans. b | Sol. : Universal Serial Bus (USB) is the most widely used interface for connecting a variety of peripheral devices due to its high speed and plug-and-play capability.

Q136. Which communication interface is commonly used for high-speed serial communication in embedded systems?
(a) RS-232
(b) USB
(c) SATA
(d) PCI
Ans. b | Sol. : USB is widely used for high-speed serial communication in embedded systems.RS-232 is a serial communication standard but is comparatively low-speed (typically up to a few hundred kbps) and is therefore not considered a high-speed interface.

Q137. What is the primary purpose of an interrupt?
(a) To increase processor clock speed
(b) To temporarily halt the current program and execute a service routine
(c) To permanently stop program execution
(d) To store data in cache memory
Ans. b | Sol. : An interrupt temporarily suspends the current execution so that the processor can respond to an urgent event by executing an Interrupt Service Routine (ISR).

Q138. Which interrupt is generated by hardware devices such as keyboards or timers?
(a) Software Interrupt
(b) Internal Interrupt
(c) Hardware Interrupt
(d) Program Interrupt
Ans. c | Sol. : Hardware interrupts are generated by external devices requesting processor attention for events such as keyboard input or timer expiration.
Q139. An exception occurs primarily due to:
(a) Power failure
(b) Keyboard input
(c) An abnormal condition during program execution
(d) Cache replacement
Ans. c | Sol. : Exceptions are internal events generated due to abnormal conditions such as division by zero, arithmetic overflow, or invalid instructions.
Q140. Which data transfer method allows the CPU to continuously monitor the status of an I/O device?
(a) Interrupt-driven I/O
(b) Polling
(c) DMA
(d) Channel I/O
Ans. b | Sol. : In polling, the CPU repeatedly checks the status of an I/O device to determine whether it is ready for data transfer.
Q141. Which mode of data transfer minimizes CPU involvement during data movement?
(a) Polling
(b) Interrupt-driven I/O
(c) Direct Memory Access (DMA)
(d) Programmed I/O
Ans. c | Sol. : DMA enables data transfer directly between memory and I/O devices without continuous CPU intervention, improving system performance.
Q142. During DMA operation, the CPU:
(a) Performs all data transfers
(b) Remains permanently idle
(c) Transfers control of the system bus to the DMA controller
(d) Disables memory access
Ans. c | Sol. : The DMA controller temporarily takes control of the system bus to perform high-speed data transfers directly between memory and peripheral devices.
Q143. Synchronous communication requires:
(a) A common clock signal between sender and receiver
(b) Start and stop bits for every character
(c) Error detection only
(d) Variable transmission speed
Ans. a | Sol. : Synchronous communication uses a shared clock to synchronize data transmission, allowing faster communication than asynchronous methods.
Q144. In asynchronous communication, synchronization is achieved using:
(a) Clock pulses
(b) Cache memory
(c) Start and stop bits
(d) Interrupt signals
Ans. c | Sol. : Asynchronous communication uses start and stop bits with each data character to synchronize transmission without requiring a shared clock.
Q145. Which standard communication interface is primarily used for connecting storage devices such as SSDs and HDDs?
(a) SATA
(b) USB
(c) HDMI
(d) VGA
Ans. a | Sol. : Serial ATA (SATA) is a high-speed communication interface specifically designed for connecting storage devices to the motherboard.
Q146. Which interface is mainly used for transmitting high-definition audio and video signals?
(a) USB
(b) Ethernet
(c) HDMI
(d) RS-232
Ans. c | Sol. : High-Definition Multimedia Interface (HDMI) transmits uncompressed digital video and audio between multimedia devices.
Q147. Which bus carries memory addresses from the CPU to memory?
(a) Data Bus
(b) Address Bus
(c) Control Bus
(d) System Bus
Ans. b | Sol. : The address bus carries the address of the memory location or I/O device that the CPU intends to access.
Q148. Which bus carries actual data between CPU, memory, and I/O devices?
(a) Address Bus
(b) Control Bus
(c) Data Bus
(d) Expansion Bus
Ans. c | Sol. : The data bus transfers actual data among the processor, memory, and peripheral devices.
Q149. The width of the address bus determines:
(a) Processor speed
(b) Number of instructions
(c) Maximum addressable memory
(d) Cache size
Ans. c | Sol. : An n-bit address bus can address up to 2^n unique memory locations, determining the maximum memory capacity.
Q150. Which memory stores the bootstrap program required to start a computer?
(a) RAM
(b) Cache
(c) ROM
(d) Register

Ans. c | Sol. : Read-Only Memory (ROM) stores firmware, including the bootstrap program used during system startup.

Q151. Which register is primarily used to store the address of the next instruction to be executed?
(a) Memory Address Register (MAR)
(b) Program Counter (PC)
(c) Instruction Register (IR)
(d) Accumulator (AC)
Ans. b | Sol. : The Program Counter (PC) always contains the memory address of the next instruction to be fetched for execution.

Q152. Which component of the Arithmetic Logic Unit is responsible for detecting arithmetic overflow?
(a) Multiplexer
(b) Flag Register
(c) Cache Memory
(d) Decoder
Ans. b | Sol. : The Flag Register stores status flags such as Carry, Zero, Sign, Overflow, and Parity that indicate the result of arithmetic and logical operations.

Q153. A processor uses a 32-bit ALU. What is the maximum unsigned decimal number that can be represented?
(a) 2,147,483,647
(b) 4,294,967,295
(c) 65,535
(d) 8,589,934,592
Ans. b | Sol. : A 32-bit unsigned number can represent values from 0 to $2^{32}-1 = 4,294,967,295$.

Q154. Which addressing mode is most suitable for implementing array traversal?
(a) Immediate Addressing
(b) Register Addressing
(c) Indexed Addressing
(d) Implied Addressing
Ans. c | Sol. : Indexed addressing efficiently accesses array elements by adding an index value to the base address.

Q155. The Control Unit of a processor is mainly responsible for
(a) Performing arithmetic calculations
(b) Storing user programs permanently
(c) Generating timing and control signals
(d) Executing input operations only
Ans. c | Sol. : The Control Unit coordinates processor operations by generating appropriate control and timing signals.

Q156. Which memory has the shortest access time?
(a) Magnetic Disk
(b) Cache Memory
(c) Main Memory
(d) Optical Disk
Ans. b | Sol. : Cache memory is built using high-speed SRAM and provides the fastest access among these memories.

Q157. Which cache mapping technique minimizes conflict misses but requires associative search?
(a) Direct Mapping
(b) Fully Associative Mapping
(c) Set Associative Mapping
(d) Sequential Mapping
Ans. b | Sol. : Fully associative mapping allows any memory block to be placed in any cache line, reducing conflict misses but increasing hardware complexity.

Q158. In a memory hierarchy, which statement is correct?
(a) Capacity decreases from disk to registers.
(b) Speed increases from registers to disk.
(c) Cost per bit increases from disk to registers.
(d) Registers have the highest capacity.
Ans. c | Sol. : Faster memories such as registers are more expensive per bit than slower storage devices like disks.

Q159. A virtual memory system primarily uses which storage device to store pages that are not currently in RAM?
(a) Cache Memory
(b) Hard Disk or SSD
(c) Register File
(d) ROM
Ans. b | Sol. : Virtual memory stores inactive pages on secondary storage such as a hard disk or SSD.

Q160. Which memory device is non-volatile and electrically erasable?
(a) SRAM
(b) DRAM
(c) EEPROM
(d) Cache
Ans. c | Sol. : EEPROM retains data without power and can be erased and reprogrammed electrically.

Q161. Which I/O technique allows the CPU to continue executing instructions while data transfer is in progress?
(a) Programmed I/O
(b) Polling
(c) Direct Memory Access (DMA)
(d) Busy Waiting
Ans. c | Sol. : DMA transfers data directly between memory and I/O devices without continuous CPU intervention.

Q162. A printer is connected through a USB interface. USB is an example of a
(a) Parallel Interface only
(b) Standard Communication Interface
(c) Memory Bus
(d) Processor Register
Ans. b | Sol. : USB is a widely accepted standard communication interface for connecting peripheral devices.

Q163. Which interrupt has the highest priority in most computer systems?
(a) Software Interrupt
(b) Maskable Interrupt

(c) Non-Maskable Interrupt (NMI)
(d) Timer Interrupt
Ans. c | Sol. : NMI cannot be disabled and is reserved for handling critical hardware failures.

Q164. An interrupt generated due to division by zero is classified as
(a) External Interrupt
(b) Software Exception
(c) DMA Interrupt
(d) I/O Interrupt
Ans. b | Sol. : Division by zero generates an internal exception because it results from instruction execution.

Q165. In vectored interrupt handling,
(a) The CPU searches all devices sequentially.
(b) The interrupting device provides the address of the Interrupt Service Routine.
(c) Interrupts cannot be nested.
(d) Polling is mandatory.
Ans. b | Sol. : In vectored interrupts, the ISR address is supplied directly, reducing interrupt response time.

Q166. Which data transfer mode is most suitable for transferring large blocks of data between memory and disk?
(a) Polling
(b) Interrupt-driven I/O
(c) DMA
(d) Programmed I/O
Ans. c | Sol. : DMA efficiently transfers large data blocks without occupying the CPU during each transfer.

Q167. During programmed I/O, the processor
(a) Transfers data independently
(b) Continuously checks device status before transferring data
(c) Uses DMA controller
(d) Never interacts with I/O devices
Ans. b | Sol. : In programmed I/O, the CPU repeatedly checks the device status register before data transfer.

Q168. Which communication method requires both sender and receiver to share a common clock?
(a) Asynchronous Communication
(b) Synchronous Communication
(c) Interrupt Communication
(d) Polling Communication
Ans. b | Sol. : Synchronous communication uses a common clock signal for coordinated data transmission.

Q169. Which feature distinguishes asynchronous communication from synchronous communication?
(a) Shared Clock
(b) Continuous Data Stream
(c) Start and Stop Bits
(d) Parallel Data Transfer
Ans. c | Sol. : Asynchronous communication uses start and stop bits instead of a shared clock.

Q170. Which standard communication interface is commonly used for long-distance serial communication?
(a) PCI Express
(b) RS-232
(c) AGP
(d) ISA Bus
Ans. b | Sol. : RS-232 is a widely used serial communication standard for long-distance data transmission.

Q171. SPI communication differs from I²C because SPI
(a) Uses only one data line
(b) Requires device addressing
(c) Supports full-duplex communication
(d) Uses start and stop conditions
Ans. c | Sol. : SPI provides separate data lines for transmission and reception, enabling simultaneous two-way communication.

Q172. Which communication interface is primarily designed for connecting high-speed storage devices inside a computer?
(a) SATA
(b) PS/2
(c) VGA
(d) RS-485
Ans. a | Sol. : SATA is a high-speed serial interface designed for connecting internal storage devices.

Q173. The primary advantage of interrupt-driven I/O over programmed I/O is that it
(a) Eliminates memory access
(b) Improves CPU utilization
(c) Removes the need for device controllers
(d) Increases memory size
Ans. b | Sol. : Interrupt-driven I/O allows the CPU to perform other tasks until an interrupt signals I/O completion.

Q174. If a DMA controller transfers 2048 bytes using a bus width of 32 bits, how many bus transfers are required?
(a) 256
(b) 512
(c) 1024
(d) 2048
Ans. b | Sol. : A 32-bit bus transfers 4 bytes at a time. Therefore, 2048 ÷ 4 = 512 bus transfers.

Q175. Which port is commonly used for Ethernet communication?
(a) RJ-45
(b) PS/2
(c) HDMI
(d) VGA
Ans. a | Sol. : RJ-45 is the standard connector used for Ethernet-based network communication.

Q176. Which of the following situations justifies the use of a microprogrammed Control Unit instead of a hardwired Control Unit?
(a) When maximum execution speed is the only objective
(b) When instruction set modifications and flexibility are required

(c) When the processor contains only combinational circuits
(d) When memory access time must be minimized
Ans. b | Sol. : A microprogrammed Control Unit is easier to modify and extend because control signals are generated through microinstructions stored in control memory. It offers greater flexibility than a hardwired Control Unit, although it is generally slower.

Q177. Which operation cannot be performed directly by a standard Arithmetic Logic Unit (ALU) without additional hardware support?
(a) Bitwise AND
(b) Integer Addition
(c) Floating-point Division
(d) Two's Complement Subtraction
Ans. c | Sol. : Standard ALUs perform integer arithmetic and logical operations. Floating-point division typically requires a dedicated Floating Point Unit (FPU) or specialized arithmetic circuitry.

Q178. A processor has separate instruction and data memories. Which architectural advantage is achieved compared to a single shared memory architecture?
(a) Increased memory latency
(b) Simultaneous instruction fetch and data access
(c) Reduced instruction throughput
(d) Elimination of cache memory
Ans. b | Sol. : Separate instruction and data memories allow simultaneous instruction fetching and data transfer, eliminating memory access conflicts and improving processor performance.

Q179. A processor executes 40% arithmetic instructions, 35% memory instructions, and 25% branch instructions. If the ALU becomes 25% faster while other operations remain unchanged, what is the overall speedup according to Amdahl's Law?
(a) 1.05
(b) 1.12
(c) 1.18
(d) 1.25
Ans. b | Sol. : Using Amdahl's Law,

$$\text{Speedup} = \frac{1}{\frac{0.40}{1.25} + 0.60}$$

$$= \frac{1}{0.32 + 0.60} = \frac{1}{0.92} \approx 1.087$$

The exact speedup is approximately 1.09.
Among the given options, 1.12 is the closest value.

Q180. Which memory organization minimizes processor stalls when executing a pipelined architecture?
(a) Single-port memory
(b) Dual-port memory
(c) ROM
(d) Sequential memory
Ans. b | Sol. : Dual-port memory allows simultaneous read/write operations, reducing contention and improving pipeline efficiency.

Q181. A cache memory uses direct mapping. Two frequently accessed memory blocks always map to the same cache line. Which performance issue will most likely occur?
(a) Spatial locality
(b) Conflict miss
(c) Capacity miss
(d) Cold miss
Ans. b | Sol. : In direct-mapped caches, multiple memory blocks mapping to the same cache location continuously replace each other, causing conflict misses.

Q182. Which interrupt should receive the highest priority in a real-time embedded system?
(a) Keyboard interrupt
(b) Timer interrupt controlling safety mechanisms
(c) Printer interrupt
(d) Disk completion interrupt
Ans. b | Sol. : Safety-critical timer interrupts require immediate servicing to maintain deterministic system behavior in real-time applications.

Q183. A processor receives an interrupt while executing another interrupt service routine. Which hardware feature allows higher-priority interrupts to be serviced immediately?
(a) DMA
(b) Interrupt nesting
(c) Polling
(d) Virtual memory
Ans. b | Sol. : Interrupt nesting allows a higher-priority interrupt to preempt a currently executing lower-priority interrupt service routine.

Q184. Which condition is classified as an exception rather than an external interrupt?
(a) Keyboard key press
(b) Mouse movement
(c) Divide-by-zero operation
(d) Network packet arrival
Ans. c | Sol. : Exceptions originate internally during instruction execution. Divide-by-zero is generated by the processor itself, unlike hardware interrupts.

Q185. A DMA controller transfers an entire data block between disk and memory. What is the primary advantage over programmed I/O?
(a) Increased processor involvement
(b) Reduced CPU utilization
(c) Higher cache miss rate
(d) Slower data transfer
Ans. b | Sol. : DMA transfers data directly between I/O devices and memory, allowing the CPU to execute other tasks concurrently.

Q186. A system continuously checks an input device until it becomes ready. Which data transfer technique is being used?
(a) DMA
(b) Interrupt-driven I/O
(c) Polling
(d) Cycle stealing

Ans. c | Sol. : Polling repeatedly checks device status, resulting in CPU time being wasted while waiting for the device.

Q187. Which data transfer method provides the highest CPU efficiency for transferring large multimedia files?
(a) Polling
(b) Interrupt-driven I/O
(c) DMA
(d) Memory-mapped I/O
Ans. c | Sol. : DMA transfers large blocks directly between memory and devices without continuous CPU intervention, maximizing processor efficiency.

Q188. A communication system sends data without using a common clock signal. Which synchronization technique is required?
(a) Parallel synchronization
(b) Start and stop bits
(c) Cache synchronization
(d) Memory synchronization
Ans. b | Sol. : Asynchronous communication uses start and stop bits to synchronize sender and receiver without a shared clock.

Q189. Which characteristic distinguishes synchronous communication from asynchronous communication?
(a) It uses parity bits only.
(b) It requires a common clock signal.
(c) It transfers one bit at a time.
(d) It does not require synchronization.
Ans. b | Sol. : Synchronous communication relies on a common clock, enabling faster and continuous data transmission.

Q190. A UART is primarily associated with which type of communication?
(a) Synchronous serial communication
(b) Asynchronous serial communication
(c) Parallel communication
(d) Optical communication
Ans. b | Sol. : UART converts parallel data into asynchronous serial format using start and stop bits.

Q191. Which interface standard provides plug-and-play support along with automatic device detection?
(a) RS-232
(b) USB
(c) Centronics
(d) PS/2
Ans. b | Sol. : USB supports automatic device detection, configuration, and hot swapping through plug-and-play functionality.

Q192. Which communication interface is most appropriate for connecting multiple industrial sensors over long distances with high noise immunity?
(a) USB
(b) RS-485
(c) HDMI
(d) PCI Express
Ans. b | Sol. : RS-485 supports long-distance communication, multiple devices, and excellent noise immunity in industrial environments.

Q193. Which interface provides the highest bandwidth for connecting modern graphics cards to the motherboard?
(a) PCI
(b) AGP
(c) PCI Express
(d) ISA
Ans. c | Sol. : PCI Express uses high-speed serial lanes and provides significantly greater bandwidth than older expansion interfaces.

Q194. Memory-mapped I/O differs from isolated I/O because memory-mapped I/O:
(a) Uses separate address space for I/O devices.
(b) Uses the same address space as main memory.
(c) Requires DMA for every operation.
(d) Does not support interrupts.
Ans. b | Sol. : Memory-mapped I/O assigns memory addresses to I/O devices, allowing standard memory instructions to access peripherals.

Q195. Which addressing technique enables faster communication between CPU and peripheral devices by reducing instruction complexity?
(a) Memory-mapped I/O
(b) Polling
(c) DMA
(d) Cache mapping
Ans. a | Sol. : Memory-mapped I/O allows the processor to use regular load/store instructions instead of specialized I/O instructions.

Q196. If an interrupt request arrives during execution of a non-interruptible machine instruction, when will the processor normally service the interrupt?
(a) Immediately
(b) After completing the current instruction
(c) During operand fetch
(d) Before instruction decoding
Ans. b | Sol. : Most processors complete the current instruction before servicing an interrupt to maintain program consistency.

Q197. A processor has an interrupt latency of 8 µs and an interrupt service routine execution time of 22 µs. What is the total interrupt handling time?
(a) 22 µs
(b) 30 µs
(c) 14 µs
(d) 176 µs
Ans. b | Sol. : Total interrupt handling time = Interrupt latency + ISR execution time = 8 + 22 = 30 µs.

Q198. Which memory type is most suitable for storing firmware that rarely changes but requires fast read access?
(a) SRAM
(b) DRAM
(c) Flash ROM

(d) Cache memory
Ans. c | Sol. : Flash ROM provides non-volatile storage with fast read access and allows firmware updates when necessary.

Q199. A computer system experiences excessive cache misses despite having sufficient cache capacity. Which cache mapping technique is most likely responsible?
(a) Fully associative mapping
(b) Set-associative mapping
(c) Direct mapping
(d) Virtual mapping
Ans. c | Sol. : Direct mapping suffers from frequent conflict misses because multiple memory blocks compete for the same cache location.

Q200. Which port is specifically designed to support high-speed video transmission with integrated audio?
(a) Serial Port
(b) HDMI
(c) PS/2
(d) RJ-11
Ans. b | Sol. : HDMI transmits high-definition digital video and audio simultaneously through a single interface.

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